REMARKS

Claims 1, 15, and 16 have been amended to clarify, as opposed to narrowing the scope of, the invention. This amendment does not add any new matter. For example, the amendments are supported in the specification within Figures 4 and 5 which illustrate multiplexing of functionally different types of receive and transmit control signals, among other places. Additionally, claims 17 and 18 recite multiplexing of different functional types of control signals. Claims 1-18 remain pending.

Rejection of Claims under §102(e) and §103(a)

The Examiner has rejected claim 16 under 35 U.S.C. §102(e) as being anticipated by Runaldue et al. (U.S. Patent No. 6,108,726). The rejection is respectfully traversed for at least the following reasons. The Examiner has also rejected claims 1-15 and 17-18 under 35 U.S.C. §103(a) as being unpatentable over Runaldue et al. in further view of Chow et al. (U.S. Patent No. 6,169,742)

Claim 1 is directed towards a "method of communicating between a media access control layer and a physical layer." Claim 1 also requires "sending a plurality of time-division multiplexed receive control signals on a receive control line" and "sending a plurality of time-division multiplexed transmit control signals on a transmit control line." Claim 1 also requires "wherein the receive control signals are functionally different types of signals and the transmit control signals are functionally different types of signals." Independent claim 15 is directed towards an "interface between a first media access control layer and a second media access control layer." Claim 15 also requires "a time-division multiplexed receive control line for transmitting different functional types of receive control signals" and "a time-division multiplexed transmit control line for transmitting different functional types of tranmit control signals." Independent claim 16 has similar elements.

Runaldue discloses a MAC to PHY interface having seven pins (wires): CLOCK, TXDATA, TXEN, COL, CRS, RXDATA, and RXDATAVALID, as shown in Fig. 3 and described at column 3, line 36 - column 4, line 3, for every four GPSI connections (ports). Six of the seven wires in the Runaldue interface are defined as "an input" or "multiplexed inputs." As shown in FIG. 5, each wire of Runaldue has a fixed function, which is used for a set of four ports or "channels." These ports or channels are for interfacing the same functional type of signal with different devices. See generally, column 3, lines 42-45: "The mulplexer interface of the preferred embodiment uses a total of 7 pins (CLOCK, TXDATA, TXEN, COL, CRS, RXDATA, and RXDATAVALID) for ever four GPSI connections." Stated another way, each of

Runaldue's wires conveys a signal having the same function (one of the seven defined in the specification as noted above) to a group of different channels or connections. Thus, Runaldue's system relates to "multiplexing by channels."

The present invention relates to time-division multiplexing done on the basis of function, thus multiplexing of functionally different control signals, rather than on the basis of channels or connections as taught by Runaldue. Instead of pins with a fixed function time-division multiplexed into multiple time slots conveying multiple signals of a given function, the present invention utilizes time-division multiplexing in which each time slot functions differently. In other words, according to the present invention, each pin (wire) has a set of functionally different signals depending on the time slot, in the manner claimed. The secondary reference Chow also fails to teach or suggest multiplexing (or a control line for multiplexing) functionally different types of signals in the manner claimed in claims 1, 15, and 16. Accordingly, it is respectfully submitted that claims 1, 15, and 16 are patentable over the cited references.

The Examiner's rejections of the dependent claims are also respectfully traversed. However, to expedite prosecution, all of these claims will not be argued separately. Claims 2-14, 17, and 18 depend directly or indirectly from independent claims 1 or 16 and, therefore, are respectfully submitted to be patentable over cited art for at least the reasons set forth above with respect to claims 1 or 15. Further, the dependent claims require additional elements that when considered in context of the claimed inventions further patentably distinguish the invention from the cited art.

Double Patenting Rejections and Provisional Rejections

Claim 16 is rejected under the judicially-created doctrine of obviousness-type double patenting as being unpatentable over claims 17-19 of U.S. Patent No. 5,953,345. Claims 1-15 are provisionally rejected under the judicially-created doctrine of obviousness-type double patenting as being unpatentable over claims 21, 26 and 31 of co-pending application No. 09/088,956.

A terminal disclaimer has been filed herein to overcome the double patenting rejections and provisional rejections.

Applicant believes that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a

telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

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APPENDIX

Claims 13, 21, 23, 24, 25, 39, and 41 have been amended as follows. All pending claims are shown, including unamended claims.

1. (Amended Twice) A method of communicating between a media access control layer and a physical layer, comprising:

sending a 100 MHz time-division multiplexed signal on a receive data line ;

sending a plurality of time-division multiplexed receive control signals on a receive control line;

sending a 100 MHz time-division multiplexed signal on a transmit data line;

sending a plurality of time-division multiplexed transmit control signals on a transmit control line,

wherein the receive control signals are functionally different types of signals and the transmit control signals are functionally different types of signals.

2 The method of claim 1 wherein the time-division multiplexed receive control signal includes 4 bit segments and wherein each 4 bit segment includes a synchronization bit.

3. The method of claim 2 wherein the receive data line includes 4 bit segments and wherein the beginning of a 4 bit segment is determined by the synchronization bit.

4. The method of claim 1 wherein the time-division multiplexed receive control signal includes 4 bit segments and wherein each 4 bit segment includes a receive data valid bit.

5. The method of claim 1 wherein the time-division multiplexed receive control signal includes 4 bit segments and wherein each 4 bit segment includes a receive error bit.

6. The method of claim 1 wherein the time-division multiplexed receive control signal includes 4 bit segments and wherein each 4 bit segment includes a carrier sense bit.

7. The method of claim 1 wherein the time-division multiplexed transmit control signal includes 4 bit segments and wherein each 4 bit segment includes a synchronization bit.

8. The method of claim 7 wherein the transmit data line includes 4 bit segments and wherein the beginning of a 4 bit segment is determined by the synchronization bit.

9. The method of claim 1 wherein the time-division multiplexed transmit control signal includes 4 bit segments and wherein each 4 bit segment includes a transmit enable bit.

10. The method of claim 1 wherein the time-division multiplexed transmit control signal includes 4 bit segments and wherein each 4 bit segment includes a transmit error bit.

11. The method of claim 1 further including indicating the speed of the PHY using the receive data line.

12. The method of claim 11 wherein indicating the speed of the PHY using the receive data line includes including an interface speed bit in a data segment when a receive control segment indicates no carrier sense, no receive data valid and no receive error.

13. The method of claim 1 further including buffering data transmitted from the PHY to the MAC using an elasticity buffer that is at least 27 bits long.

14. The method of claim 1 further including buffering data transmitted from the PHY to the MAC using an elasticity buffer that long enough to buffer an entire frame of data from a data source having a clock with a frequency tolerance of 0.1%.

15. (Amended Twice) An interface between a first media access control layer and a second media access control layer, consisting essentially of:

a time-division multiplexed receive data line;

a time-division multiplexed receive control line for transmitting different functional types of receive control signals;

a time-division multiplexed transmit data line;

a time-division multiplexed transmit control line for transmitting different functional types of receive control signals.

16. (Amended Twice) A media access control layer to physical layer interface consisting essentially of:

a common clock;

a time-division multiplexed receive data line;

a time-division multiplexed receive control line for transmitting different functional types of receive control signals;

a time-division multiplexed transmit data line;

a time-division multiplexed transmit control line for transmitting different functional types of receive control signals.

17. The interface of claim 16, wherein said time-division multiplexed receive control line contains signals comprising a receive date valid signal, a receive error signal and a carrier sense signal.

18. The interface of claim 16, wherein said time-division multiplexed transmit control line contains signals comprising a transmit enable signal and a transmit error signal.